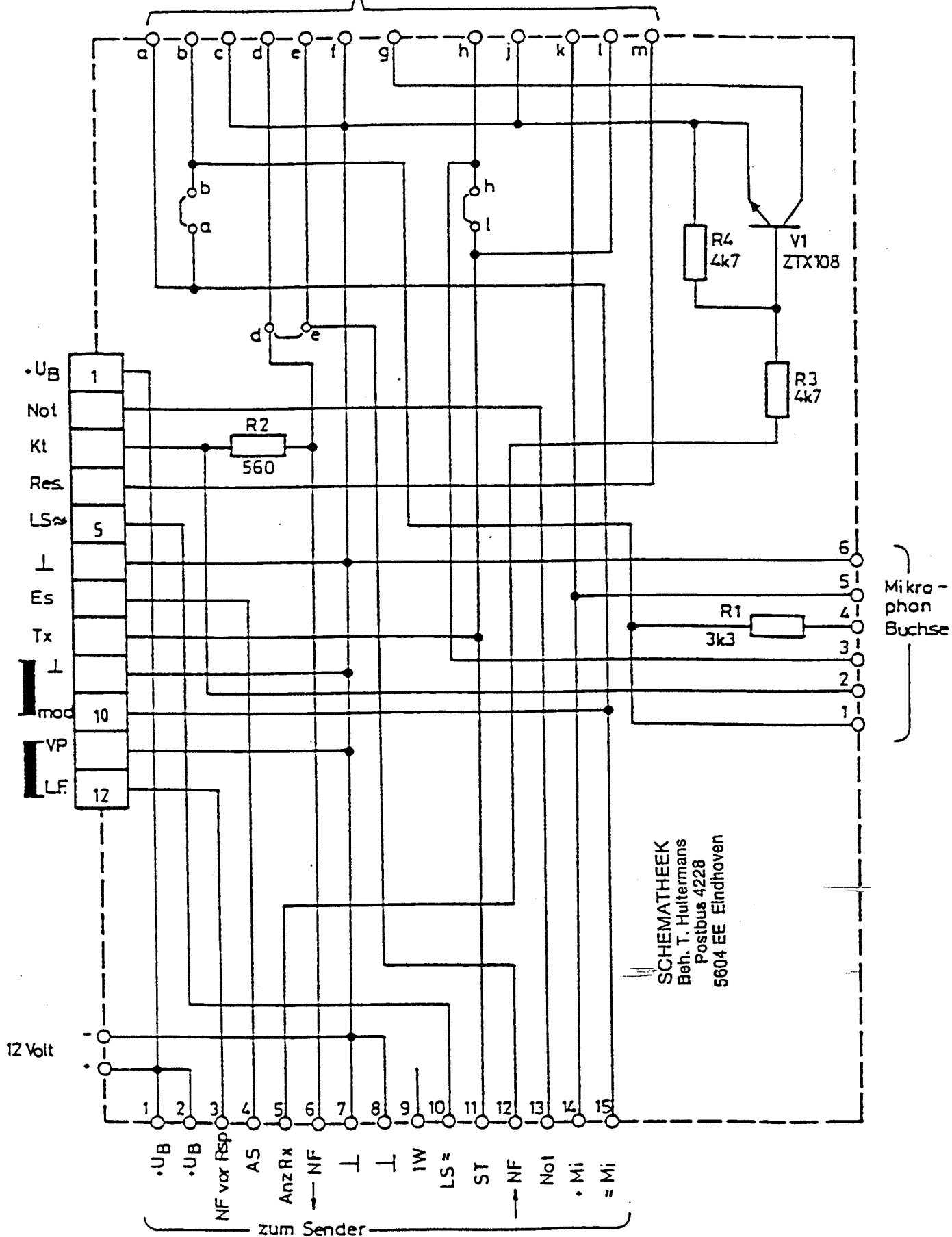


PVD - Buchse

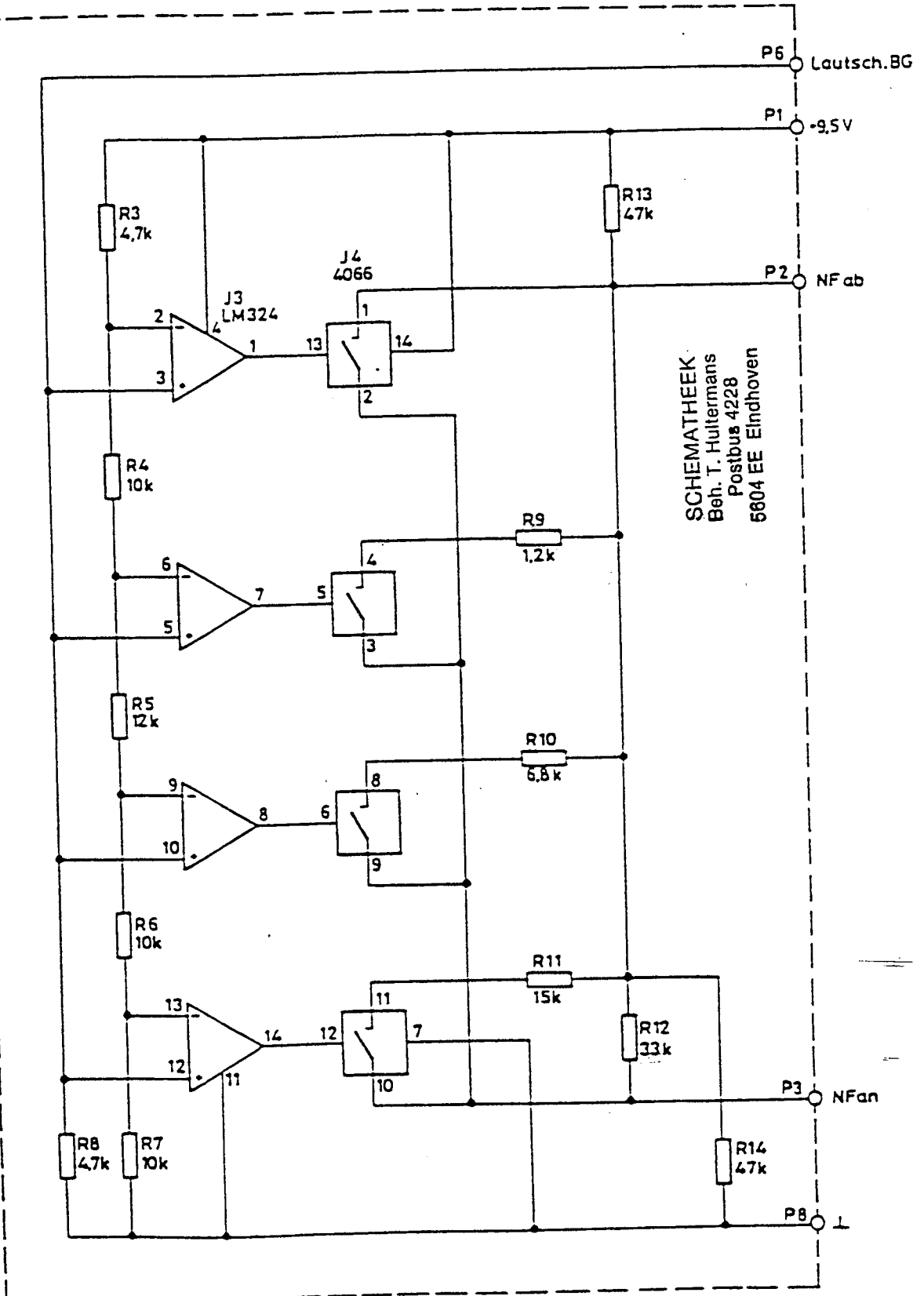


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 Beh. T. Hultermans  
 Postbus 4228  
 5604 EE Eindhoven

Tag	Name
Bearb. 11.2.85	<i>[Signature]</i>
Geor.	
Heinrich Pfitzner	

PVD - Anschaltung

mit Genehmigung von...  
 g. unaut. Wettbewerb BCB  
 ...



SCHEMATHEEK  
 Beh. T. Hultermans  
 Postbus 4228  
 5804 EE Eindhoven

Lp.Nr. 46816.49.501

Tag	Name
Bearb. 11.3.95	Rill
Gepr.	
Heinrich Pfitzner	

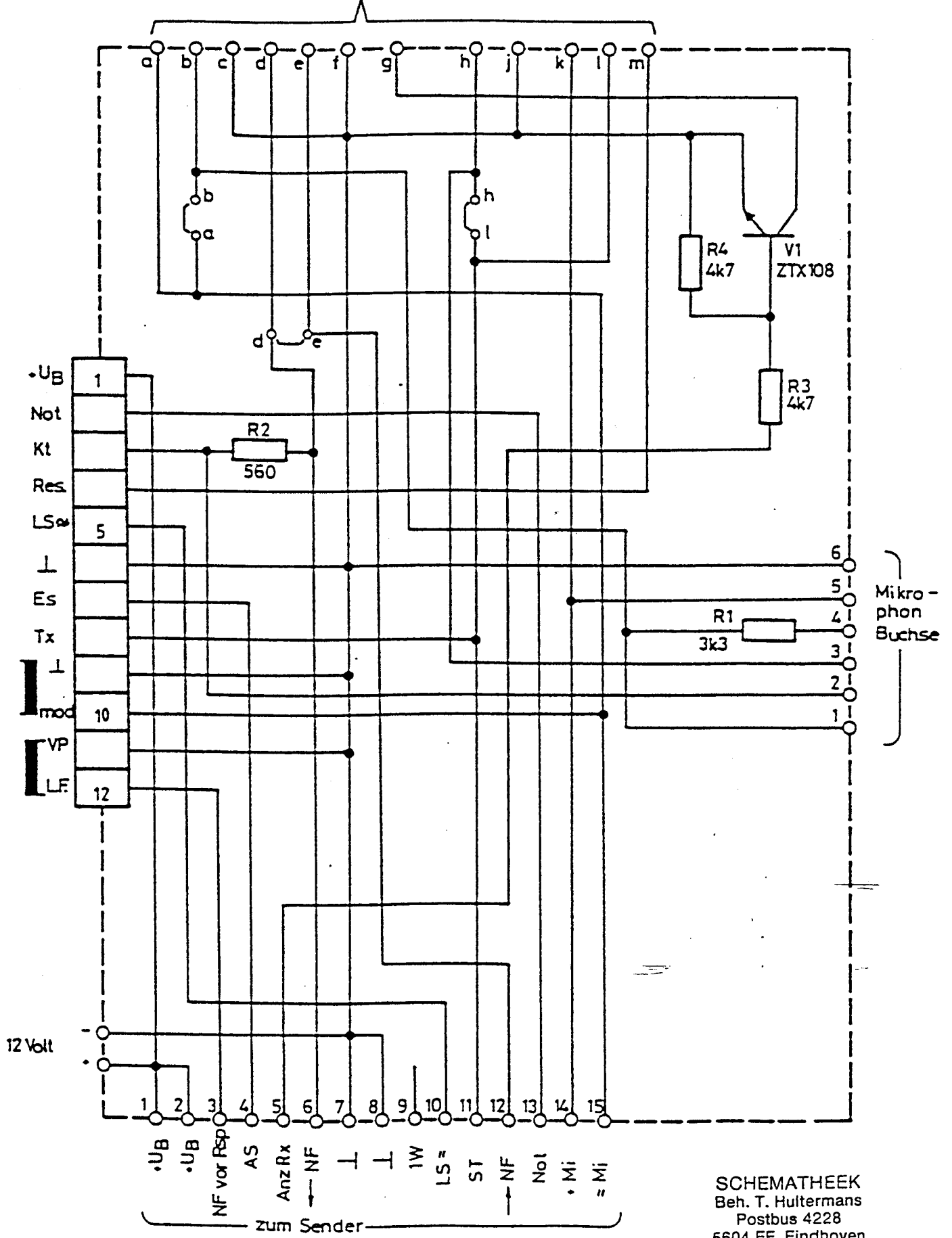
Lautstärkekoppler

TMC DVD

46816.41.501

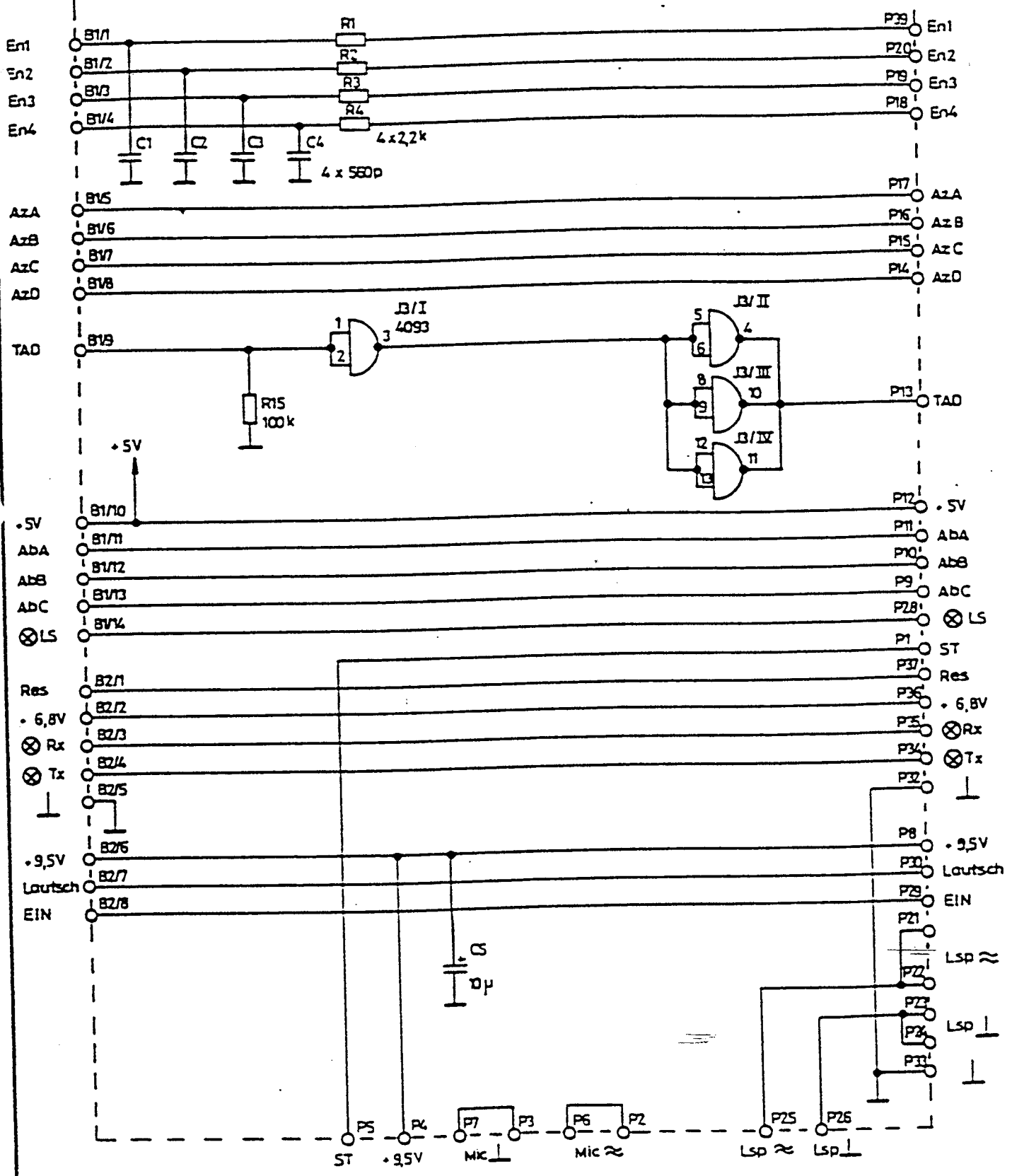
In 1999, V. 19.0. Hierin -  
 wenn ist strafbar. J wird gerichtlich verfolgt!  
 (Missbrauch, Gesetz geg unfaul Wettbewerb BCB)

PVD - Buchse



Tag	Name
Bearb. 11.2.85	<i>Tux</i>
Gepr.	
Heinrich Pfitzner	

PVD - Anschaltung



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Lp.-Nr. 46811.39.501

Tag	Name
Bearb. 73.5.24	36H
Gepr.	
Heinrich Pfitzner	

BG-Adapter

TMC. PVD | 468.11.41.501

d wird gerichtlich verfolgt.  
 sonen ist strafrechtlich  
 echtsgeheim, O.

## 80C48/80C35/80C49/80C39 CHMOS SINGLE-COMPONENT 8-BIT MICROCOMPUTER

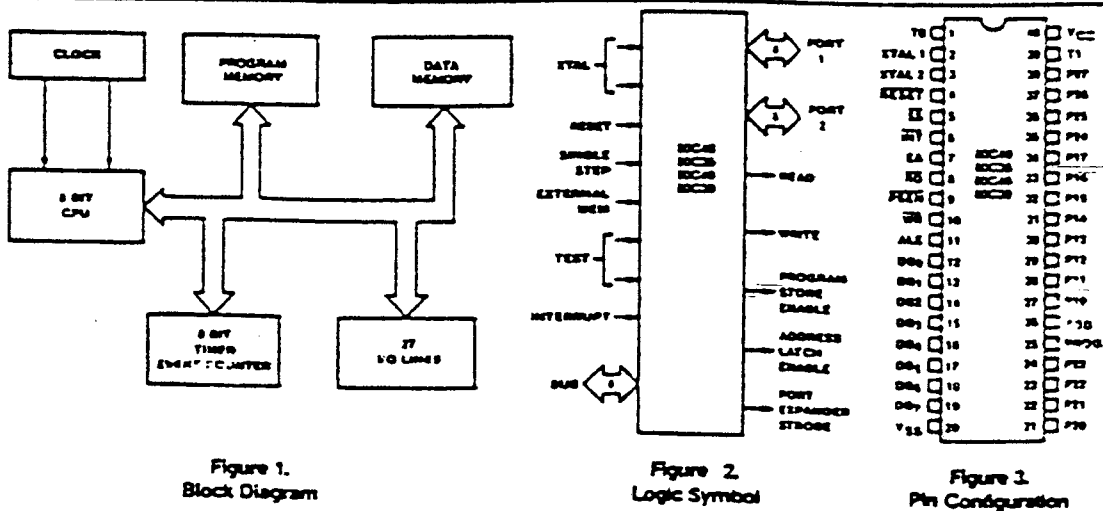
- 80C48/80C49 Low Power Mask Programmable ROM
- 80C35/80C39 Low Power, CPU only

- Pin-to-pin compatible with Intel's 8048/8035HL/8049H/8039HL
- 1.38  $\mu$ sec Instruction Cycle. All instructions 1 or 2 cycles
- Ability to maintain operation during AC power line interruptions
- Exit idle mode with an external or internal interrupt signal
- Battery Operation
- 3 power consumption selections
  - Normal Operation: 15mA @ 11 MHz @ 5V
  - Idle Mode: 500  $\mu$ A @ 11 MHz @ 5V
  - Power down: 10  $\mu$ A @ 2.0V
- 11 MHz, TTL compatible operation; VCC = 5V  $\pm$  10%  
 CMOS compatible operation; VCC = 5V  $\pm$  20%

Intel's 80C48/80C35/80C49/80C39 are low power, CHMOS versions of the popular MCS-48 HMOS family members. CHMOS is a technology built on HMOS II and features high resistivity P substrate, diffused N well, and scaled N and P channel devices. The 80C48/80C35/80C49/80C39 have been designed to provide low power consumption and high performance.

The 80C48/80C49 contains a 1K x 8/2K x 8 program memory, a 64 x 8/128 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to an on-board oscillator and clock circuits. For systems that require extra capability, the 80C48/80C49 can be expanded using CMOS external memories and MCS-80<sup>®</sup> and MCS-85<sup>®</sup> peripherals. The 80C35/80C39 is the equivalent of the 80C48/80C49 without program memory on-board.

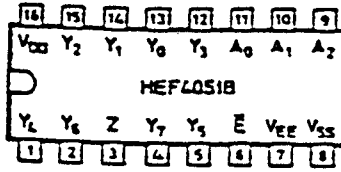
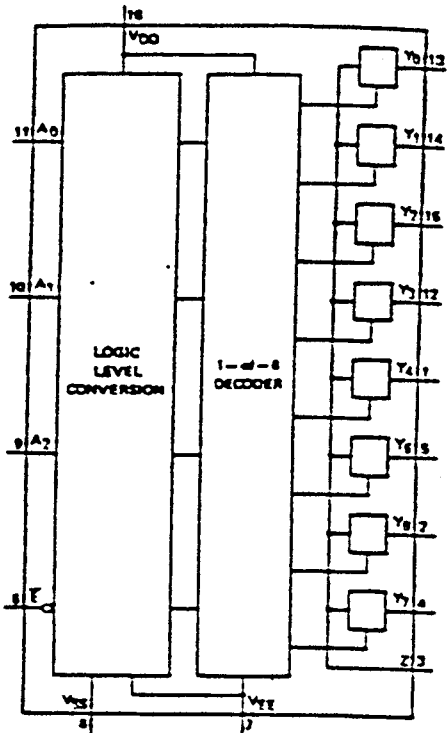
The CHMOS design of the 80C48/80C49 opens new application areas that require battery operation, low power standby, wide voltage range, and the ability to maintain operation during AC power line interruptions. These applications include portable and hand-held instruments, telecommunications, consumer, and automotive.



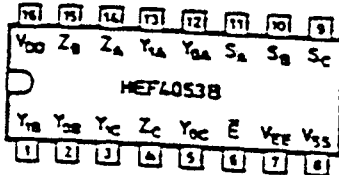
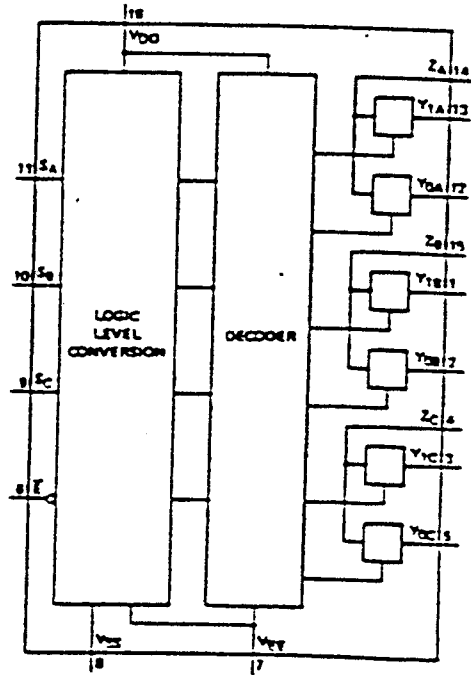
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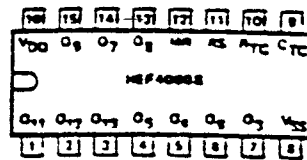
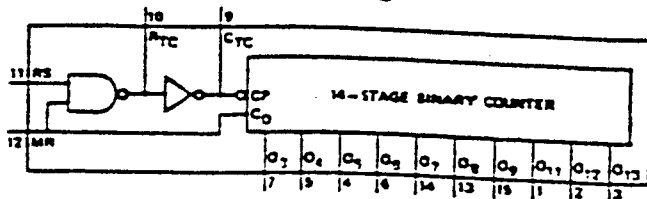


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HEF40608



Funktionsdiagramme und Anschluß-Belegungen von LOGIC IC's